Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **QL**
2. **QM**
3. **QN**
4. **QF**
5. **QE**
6. **QG**
7. **QD**
8. **GND**
9. **CK0**
10. **N. CK0**
11. **CK1**
12. **CLR**
13. **QI**
14. **QH**
15. **QJ**
16. **VCC**

**HC 4060T**

**DIE ID**

**13 12 11**

**10**

**9**

**8**

**7**

**6**

**3 4 5**

**14**

**15**

**16**

**1**

**2**

**.071”**

**.058”**

**Top Material: Al**

**Backside Material: Si Ni**

**Bond Pad Size: .0033” X .0033”**

**Backside Potential: VCC**

**Mask Ref: HC4060T**

**APPROVED BY: DK DIE SIZE .058” X .071” DATE: 3/14/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HC4060**

**DG 10.1.2**

#### Rev B, 7/19/02